IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

detecting one or more variations within a clock domain of a plurality of clock domains of a processor; [[and]]

adjusting a clock signal of the clock domain in response to the one or more variations;

comparing a speculative output of a pipeline stage of the processor with a correct output of the pipeline stage of the processor; and

determining whether the speculative output matches the correct output.

2. (Original) The method of claim 1, wherein detecting the one or more variations comprises sensing one or more of a semiconductor manufacturing process variation, operating voltage variation, temperature variation, or input value variation.

3. (Original) The method of claim 1, wherein adjusting the clock signal of the clock domain comprises adjusting a frequency of the clock signal.

4. (Original) The method of claim 1, wherein adjusting the clock signal is performed based on comparison of a threshold value with a number of timing errors detected in the clock domain.

5. (Original) The method of claim 1, further comprising synchronizing communication among the plurality of clock domains.

6. (Canceled) ~~The method of claim 1, further comprising:~~

~~comparing a speculative output of a pipeline stage with an expected output from the pipeline stage; and~~

~~determining whether the speculative output matches the expected output.~~

7. (Currently Amended) The method of claim [[6]] 1, further comprising generating an error signal if the speculative output is different than the ~~expected~~ correct output.

8. (Currently Amended) The method of claim [[6]] 1, further comprising re-executing one or more consumer instructions if the speculative output is different than the ~~expected~~ correct output.

9. (Currently Amended) An apparatus comprising:

logic to detect one or more variations within a clock domain of a plurality of clock domains of a processor; [[and]]

a frequency controller to adjust a clock signal of the clock domain in response to the one or more variations; and

a comparison logic to compare a speculative output of a pipeline stage of the processor with a correct output of the pipeline stage of the processor to determine whether the speculative output matches the correct output.

10. (Original) The apparatus of claim 9, wherein the logic to detect the one or more variations comprises one or more sensors.

11. (Original) The apparatus of claim 10, wherein the one or more sensors are one or more of a temperature sensor, a voltage droop probe, or a ring oscillator.

12. (Original) The apparatus of claim 9, wherein the logic to detect the one or more variations detects the one or more variations based on a number of detected errors within the clock domain.

13. (Original) The apparatus of claim 9, wherein the plurality of clock domains of the processor comprise one or more of a frontend domain, a backend domain, and a second level cache domain.

14. (Original) The apparatus of claim 13, wherein the frontend domain comprises one or more of a frontend sensor, a frontend frequency controller, a reorder buffer, a rename and steer unit, a trace cache, an instruction fetch unit, a decode unit, a sequencer, or a branch prediction unit.

15. (Original) The apparatus of claim 13, wherein the backend domain comprises one or more of a first level cache domain and one or more execution domains.

16. (Original) The apparatus of claim 15, wherein the first level cache domain comprises one or more of a first level cache, a first level cache frequency controller, or a first level cache sensor.

17. (Original) The apparatus of claim 15, wherein the one or more execution domains comprise one or more of an integer execution domain or a floating point execution domain.

18. (Original) The apparatus of claim 15, wherein each of the execution domains comprises one or more of an issue queue, a register file, an execution domain frequency controller, an execution domain sensor, or an execution unit.

19. (Original) The apparatus of claim 15, further comprising an interconnection to couple one or more of the first level cache domain, the one or more execution domains, or the frontend domain.

20. (Original) The apparatus of claim 9, further comprising a plurality of first-in, first-out buffers to synchronize communication among the plurality of clock domains.

21. (Original) The apparatus of claim 9, wherein the processor comprises a plurality of cores on a same die.

22. (Canceled) ~~The apparatus of claim 9, further comprising a comparison logic to compare a speculative output of a pipeline stage with an expected output from the pipeline stage to determine whether the speculative output matches the expected output.~~

23. (Currently Amended) The apparatus of claim [[22]] 9, further comprising a first storage unit to store the speculative output in response to a first clock edge and a second storage unit to store the correct output in response to a second clock edge.

24. (Original) The apparatus of claim 23, wherein the first and second clock edges are edges of the clock signal.

25. (Currently Amended) A processor comprising:

a first domain to receive a first clock signal;

a second domain to receive a second clock signal;

one or more sensors to detect one or more variations within the first domain and the second domain;

a first logic to adjust a frequency of the first clock in response to the one or more variations within the first domain; [[and]]

a second logic to adjust a frequency of the second clock in response to the one or more variations within the second domain; and

a comparison logic to compare a speculative output of a pipeline stage of the processor with a correct output of the pipeline stage of the processor to determine whether the speculative output matches the correct output.

26. (Canceled) ~~The processor of claim 25, further comprising a comparison logic to compare a speculative output of a pipeline stage of the processor with an expected output from the pipeline stage to determine whether the speculative output matches the expected output.~~

27. (Original) The processor of claim 25, further comprising one or more buffers to synchronize communication between the first and second domains.

28. (Currently Amended) A computing system comprising:

one or more domains, each domain comprising:

logic to perform one or more computing functions;

one or more sensors coupled to one or more components of the logic to perform the one or more computing functions, the one or more sensors to sense variations within a corresponding domain; [[and]]

a frequency controller coupled to the logic to perform the one or more computing functions and the one or more sensors, the frequency controller to adjust a frequency

of a clock signal for the corresponding domain in response to one or more of timing errors or variations; and

a comparison logic to compare a speculative output of a pipeline stage of a processor with a correct output of the pipeline stage of the processor to determine whether the speculative output matches the correct output.

29. (Original) The computing system of claim 28, wherein the one or more computing functions comprise one or more of data processing, data storage, and data communication.

30. (Original) The computing system of claim 28, wherein the computing system comprises at least one computing device selected from a group comprising of a personal digital assistant (PDA), a mobile phone, a laptop computer, a desktop computer, a server computer, and a workstation.